Remarks:

This is in response to the final Office Action dated March 15, 2007. Applicant files a request for continued examination with this amendment. Applicant amends claim 18. Claims 18-23 are pending. Reexamination and reconsideration are respectfully requested.

The Office Action objected to the drawings. Specifically, the Office Action states that claim 18 recites a decoder processing two substreams, one after another, but that this feature of claim 18 is not shown in the drawings. Applicant respectfully submits that the drawings illustrate this aspect of claim 18. Specifically, FIGS. 5A and 5B illustrate an embodiment in which the decoder processes two substreams (see FIG. 5A "Judgment: One or Two substreams.") and the two substreams are processed one after another. The processing of two substreams, one after another, is illustrated on the right hand side flow of FIGS. 5A and 5B (two blocks joined through node "B"). Applicant consequently submits that FIGS. 5A and 5B illustrate claim 18's recitation of:

> "the decoder core decodes the depacketized access unit for a first substream of the access unit ..., and the decoder core decodes the depacketized access unit for a second substream ...."

Applicant respectfully requests withdrawal of the objection to the drawings.

The Office Action rejects claims 18-23 as not being enabled (35 U.S.C. § 112, ¶ 1). Applicant amends claim 18 to clarify the subject matter of the claim, shifting the focus of the claim and broadening the claim. Support for this amendment is found at 7, lines 16-24 of the application. Applicant submits that the application fully supports the invention defined by claim 18, as amended. Specifically, amended claim 18 recites in part, "wherein the depacketized access unit is transmitted directly to the decoder core without accessing an external memory device for buffering...." The term "without buffering" here indicates that an

external memory device like a DRAM or FIFO is not used as a buffer for transmitting the depacktized access unit between the depacketizer and the decoder.

Page 9, lines 20-23 of the specification state:

"[P]referably no buffering is provided between the depacketizer and the decoder cores. In a preferred implementation of this decoder, the depacketizer is defined within a digital signal processor (DSP) and the one or more decoder core is defined within the same DSP. In this way, data pass from the depacketizer to the decoder cores without exiting the DSP and without accessing DRAM or FIFO external to the DSP."

Consequently, the application fully supports the subject matter of claim 18 and provides teachings sufficient that one skilled in the art would know how to implement a system according to amended claim 18 without undue experimentation. Applicant respectfully submits that claim 18 and its dependent claims 19-23 are fully supported by the application. Applicant respectfully requests reconsideration of the rejection under 35 U.S.C. § 112 and withdrawal of that rejection.

The Office Action rejects claims 18-22 as anticipated by applicant's related art discussion. In support of this rejection, the Office Action cites application page 4, lines 4-7, which states, "[i]f there are two substreams, the decoder core 0 is active when only basic reproduction is desired and both decoder core 0 and decoder core 1 are active when additional channels are processed." Based on that citation, the Office Action concludes that the related art describes a single decoder core that handles two or more substreams. Applicant respectfully disagrees. If there are two substreams, each of the two substreams is loaded into a FIFO associated with the respective decoder core 0 or decoder core 1. If only "basic reproduction" is desired, what is stored in the FIFO for decoder core 1 is ignored and eventually discarded.

The passage at page 4, lines 4-7 cited by the Office Action describes FIG. 2 of the application. FIG. 2 accurately illustrates what happens in the decoder cores and clearly illustrates that there are two FIFOs for storing two substreams respectively. Both substreams are loaded into FIFOs: "For each substream in the two FIFOs." Only one substream is directed to decoder core 0. If the decoder core 1 is not active, the substream directed to the decoder 1 is not decoded and that is what happens "*when only basic reproduction is desired*" because only one substream and not two substreams is decoded.

In contrast, claim 18 recites a playback system with one decoder core for decoding two or more than two substreams. Claim 18 recites:

> 18. A playback system for playing audio data from a storage device, the audio data containing an access unit, the playback system comprising:
>
> a system circuit for determining a number of substreams present in the access unit;
>
> a depacketizer circuit coupled to the system circuit for depacktizing the access unit; and
>
> a decoder core, wherein the depacketized access unit is transmitted directly to the decoder core without accessing to an external memory device for buffering, the decoder core decodes the depacketized access unit for a first substream of the access unit if the number of the substreams is more than one, and the decoder core decodes the depacketized access unit for a second substream of the access unit after the first substream is decoded if the number of the substream is more than one.

Claim 18 thus recites a decoder core that decodes a second substream after the first substream under certain circumstances. This is different from the background discussion of the related art, which does not describe one decoder

decoding two substreams. Consequently, claim 18 distinguishes over the background related art discussed in the application and is in condition for allowance. None of the references of record address this deficiency in the related art discussion and so claim 18 and its dependent claims 19-23 distinguish over the art of record and are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4600 to discuss the steps necessary for placing the application in condition for allowance.

Applicant has requested to charge deposit account 50-1314 in the amount of $790.00 for RCE fee. If there are any additional fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: June 15, 2007

By: _____
William H. Wright
Registration No. 36,312
Attorney for Applicants

1999 Avenue of the Stars, Suite 1400
Los Angeles, California 90067
Phone: 310-785-4600
Fax: 310-785-4601